




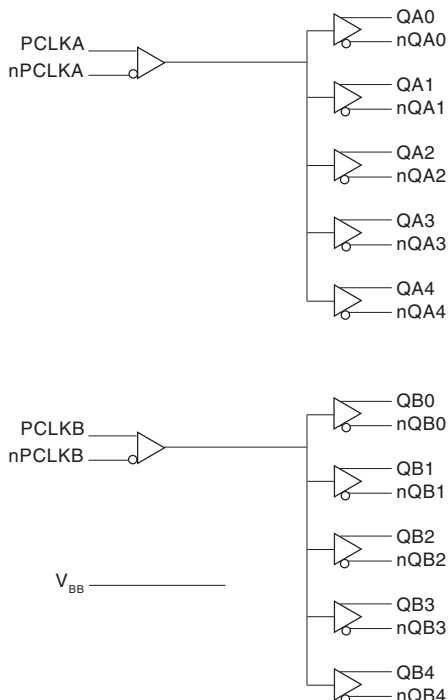
GENERAL DESCRIPTION

 The ICS853210 is a low skew, high performance dual 1-to-5 Differential-to-2.5V/3.3V LVPECL/ECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS853210 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS853210 ideal for those clock distribution applications demanding well defined performance and repeatability.

FEATURES

- 2 differential 2.5V/3.3V LVPECL / ECL bank outputs
- 2 differential clock input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: >3GHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nPCLKx input
- Output skew: 13ps (typical)
- Part-to-part skew: 85ps (typical)
- Propagation delay: 485ps (typical)
- LVPECL mode operating voltage supply range: $V_{CC} = 2.375V$ to $3.8V$, $V_{EE} = 0V$
- ECL mode operating voltage supply range: $V_{CC} = 0V$, $V_{EE} = -2.375V$ to $-3.8V$
- $-40^{\circ}C$ to $85^{\circ}C$ ambient operating temperature
- Pin compatible with MC100EP210 and MC100LVEP210

BLOCK DIAGRAM



PIN ASSIGNMENT

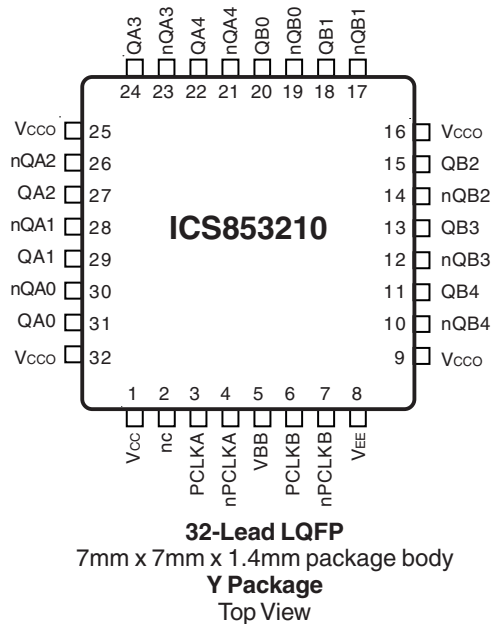




TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|-----------|------------------|--------|---------------------|---|
| 1 | V _{CC} | Power | | Core supply pin. |
| 2 | nc | Unused | | No connect. |
| 3 | PCLKA | Input | Pulldown | Non-inverting differential clock input. |
| 4 | nPCLKA | Input | Pullup/ Pulldown | Clock input. V _{CC} /2 default when left floating. |
| 5 | V _{BB} | Output | | Bias voltage. |
| 6 | PCLKB | Input | Pulldown | Non-inverting differential clock input. |
| 7 | nPCLKB | Input | Pullup/ Pulldown | Clock input. V _{CC} /2 default when left floating. |
| 8 | V _{EE} | Power | | Negative supply pin. |
| 9, 25, 32 | V _{CCO} | Power | | Output supply pins. |
| 10, 11 | nQB4, QB4 | Output | | Differential output pair. LVPECL interface levels. |
| 12, 13 | nQB3, QB3 | Output | | Differential output pair. LVPECL interface levels. |
| 14, 15 | nQB2, QB2 | Output | | Differential output pair. LVPECL interface levels. |
| 17, 18 | nQB1, QB1 | Output | | Differential output pair. LVPECL interface levels. |
| 19, 20 | nQB0, QB0 | Output | | Differential output pair. LVPECL interface levels. |
| 21, 22 | nQA4, QA4 | Output | | Differential output pair. LVPECL interface levels. |
| 23, 24 | nQA3, QA3 | Output | | Differential output pair. LVPECL interface levels. |
| 26, 27 | nQA2, QA2 | Output | | Differential output pair. LVPECL interface levels. |
| 28, 29 | nQA1, QA1 | Output | | Differential output pair. LVPECL interface levels. |
| 30, 31 | nQA0, QA0 | Output | | Differential output pair. LVPECL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|---------------------------|-----------------|---------|---------|---------|-------|
| R _{PULLDOWN} | Input Pulldown Resistor | | | 75 | | KΩ |
| R _{VCC/2} | Pullup/Pulldown Resistors | | | 50 | | KΩ |

TABLE 3. CLOCK INPUT FUNCTION TABLE

| Inputs | | Outputs | | Input to Output Mode | Polarity |
|----------------|------------------|------------------|----------------------|------------------------------|---------------|
| PCLKA or PCLKB | nPCLKA or nPCLKB | QA0:QA4, QB0:QB4 | nQA0:nQA4, nQB0:nQB4 | | |
| 0 | 1 | LOW | HIGH | Differential to Differential | Non Inverting |
| 1 | 0 | HIGH | LOW | Differential to Differential | Non Inverting |
| 0 | Biased; NOTE 1 | LOW | HIGH | Single Ended to Differential | Non Inverting |
| 1 | Biased; NOTE 1 | HIGH | LOW | Single Ended to Differential | Non Inverting |
| Biased; NOTE 1 | 0 | HIGH | LOW | Single Ended to Differential | Inverting |
| Biased; NOTE 1 | 1 | LOW | HIGH | Single Ended to Differential | Inverting |

NOTE 1: Please refer to the Application Information, "Wiring the Differential Input to Accept Single Ended Levels".



ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------------------------|
| Supply Voltage, V_{CC} | 4.6V (LVPECL mode, $V_{EE} = 0$) |
| Negative Supply Voltage, V_{EE} | -4.6V (ECL mode, $V_{CC} = 0$) |
| Inputs, V_I (LVPECL mode) | -0.5V to $V_{CC} + 0.5V$ |
| Inputs, V_I (ECL mode) | 0.5V to $V_{EE} - 0.5V$ |
| Outputs, I_O | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| V_{BB} Sink/Source, I_{BB} | $\pm 0.5mA$ |
| Operating Temperature Range, T_A | -40°C to +85°C |
| Storage Temperature, T_{STG} | -65°C to 150°C |
| Package Thermal Impedance, θ_{JA} (Junction-to-Ambient) | 47.9°C/W (0 lfpm) |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = 3.3V$; $V_{EE} = 0V$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|----------------------|-----------------|---------|---------|---------|-------|
| V_{CC} | Core Supply Voltage | | 2.375 | 3.3 | 3.8 | V |
| I_{EE} | Power Supply Current | | | | 80 | mA |

TABLE 4B. LVPECL DC CHARACTERISTICS, $V_{CC} = 3.3V$; $V_{EE} = 0V$

| Symbol | Parameter | -40°C | | | 25°C | | | 85°C | | | Units |
|-----------|--|----------------|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{OH} | Output High Voltage; NOTE 1 | 2.175 | 2.275 | 2.38 | 2.225 | 2.295 | 2.37 | 2.295 | 2.33 | 2.365 | V |
| V_{OL} | Output Low Voltage; NOTE 1 | 1.405 | 1.545 | 1.68 | 1.425 | 1.52 | 1.615 | 1.44 | 1.535 | 1.63 | V |
| V_{IH} | Input High Voltage(Single-Ended) | 2.075 | | 2.36 | 2.075 | | 2.36 | 2.075 | | 2.36 | V |
| V_{IL} | Input Low Voltage(Single-Ended) | 1.43 | | 1.765 | 1.43 | | 1.765 | 1.43 | | 1.765 | V |
| V_{BB} | Output Voltage Reference; NOTE 2 | 1.86 | | 1.98 | 1.86 | | 1.98 | 1.86 | | 1.98 | V |
| V_{PP} | Peak-to-Peak Input Voltage | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| V_{CMR} | Input High Voltage Common Mode Range; NOTE 3, 4 | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| I_{IH} | Input High Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input Low Current | PCLK0, PCLK1 | -10 | | -10 | | | -10 | | | μA |
| | | nPCLK0, nPCLK1 | -150 | | -150 | | | -150 | | | μA |

Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

NOTE 2: Single-ended input operation is limited. $V_{CC} \geq 3V$ in LVPECL mode.

NOTE 3: Common mode voltage is defined as V_{IH} .

NOTE 4: For single-ended applications, the maximum input voltage for PCLK0, nPCLK0 and PCLK1, nPCLK1 is $V_{CC} + 0.3V$.



TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{CC} = 2.5V$; $V_{EE} = 0V$

| Symbol | Parameter | -40°C | | | 25°C | | | 85°C | | | Units |
|-----------|--|--------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{OH} | Output High Voltage; NOTE 1 | 1.375 | 1.475 | 1.58 | 1.425 | 1.495 | 1.57 | 1.495 | 1.53 | 1.565 | V |
| V_{OL} | Output Low Voltage; NOTE 1 | 0.605 | 0.745 | 0.88 | 0.625 | 0.72 | 0.815 | 0.64 | 0.735 | 0.83 | V |
| V_{IH} | Input High Voltage(Single-Ended) | 1.275 | | 1.56 | 1.275 | | 1.56 | 1.275 | | -0.83 | V |
| V_{IL} | Input Low Voltage(Single-Ended) | 0.63 | | 0.965 | 0.63 | | 0.965 | 0.63 | | 0.965 | V |
| V_{PP} | Peak-to-Peak Input Voltage | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| V_{CMR} | Input High Voltage Common Mode Range; NOTE 2, 3 | 1.2 | | 2.5 | 1.2 | | 2.5 | 1.2 | | 2.5 | V |
| I_{IH} | Input High Current | PCLK0, PCLK1 nPCLK0, nPCLK1 | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input Low Current | PCLK0, PCLK1 | | -10 | | | -10 | | | -10 | μA |
| | | nPCLK0, nPCLK1 | | -150 | | | -150 | | | -150 | μA |

Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

NOTE 2: Common mode voltage is defined as V_{IH} .

NOTE 3: For single-ended applications, the maximum input voltage for PCLK0, nPCLK0 and PCLK1, nPCLK1 is $V_{CC} + 0.3V$.

TABLE 4D. ECL DC CHARACTERISTICS, $V_{CC} = 0V$; $V_{EE} = -2.375$ TO $-3.8V$

| Symbol | Parameter | -40°C | | | 25°C | | | 85°C | | | Units |
|-----------|--|--------------------------------|--------|--------|---------------|--------|--------|---------------|--------|--------|---------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{OH} | Output High Voltage; NOTE 1 | -1.125 | -1.025 | -0.92 | -1.075 | -1.005 | -0.93 | -1.005 | -0.97 | -0.935 | V |
| V_{OL} | Output Low Voltage; NOTE 1 | -1.895 | -1.755 | -1.62 | -1.875 | -1.78 | -1.685 | -1.86 | -1.765 | -1.67 | V |
| V_{IH} | Input High Voltage(Single-Ended) | -1.225 | | -0.94 | -1.225 | | -0.94 | -1.225 | | -0.94 | V |
| V_{IL} | Input Low Voltage(Single-Ended) | -1.87 | | -1.535 | -1.87 | | -1.535 | -1.87 | | -1.535 | V |
| V_{BB} | Output Voltage Reference; NOTE 2 | -1.44 | | -1.32 | -1.44 | | -1.32 | -1.44 | | -1.32 | V |
| V_{PP} | Peak-to-Peak Input Voltage | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| V_{CMR} | Input High Voltage Common Mode Range; NOTE 3, 4 | $V_{EE}+1.2V$ | | 0 | $V_{EE}+1.2V$ | | 0 | $V_{EE}+1.2V$ | | 0 | V |
| I_{IH} | Input High Current | PCLK0, PCLK1 nPCLK0, nPCLK1 | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input Low Current | PCLK0, PCLK1 | | -10 | | | -10 | | | -10 | μA |
| | | nPCLK0, nPCLK1 | | -150 | | | -150 | | | -150 | μA |

Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

NOTE 2: Single-ended input operation is limited. $V_{CC} \geq 3V$ in LVPECL mode.

NOTE 3: Common mode voltage is defined as V_{IH} .

NOTE 4: For single-ended applications, the maximum input voltage for PCLK0, nPCLK0 and PCLK1, nPCLK1 is $V_{CC} + 0.3V$.



TABLE 5. AC CHARACTERISTICS, $V_{CC} = 0V$; $V_{EE} = -2.375$ TO $-3.8V$ OR $V_{CC} = 2.375$ TO $3.8V$; $V_{EE} = 0V$

| Symbol | Parameter | -40°C | | | 25°C | | | 85°C | | | Units | | |
|---------------|--|------------|-----|-----|------|-----|-----|------|-----|-----|-------|-----|----|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | | |
| f_{MAX} | Output Frequency | | >3 | | | >3 | | | >3 | | GHz | | |
| $t_{P_{LH}}$ | Propagation Delay, Low-to-High; NOTE 1 | 415 | 470 | 520 | 430 | 485 | 545 | 435 | 515 | 585 | ps | | |
| $t_{P_{HL}}$ | Propagation Delay, High-to-Low; NOTE 1 | @ 2.5V | | 400 | 470 | 540 | 425 | 490 | 550 | 445 | 515 | 585 | ps |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 4 | | 13 | 25 | | 13 | 25 | | 13 | 25 | ps | | |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | 85 | 160 | | 85 | 160 | | 85 | 160 | ps | | |
| t_{R}/t_{F} | Output Rise/Fall Time | 20% to 80% | | 115 | 188 | 260 | 130 | 190 | 250 | 145 | 190 | 235 | ps |

All parameters tested ≤ 1 GHz unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

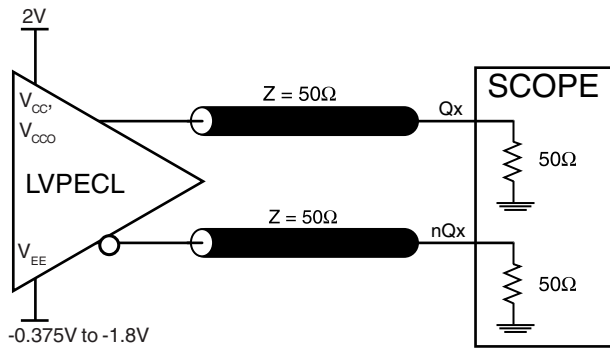
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

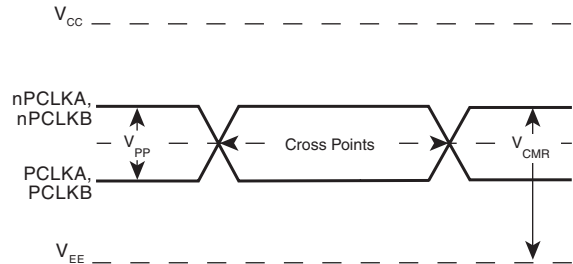
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



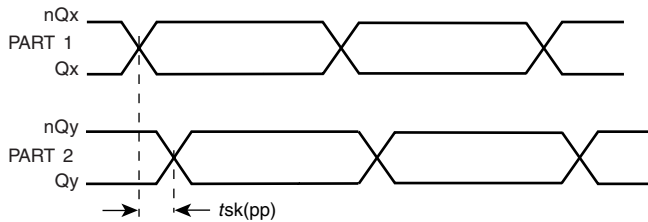
PARAMETER MEASUREMENT INFORMATION



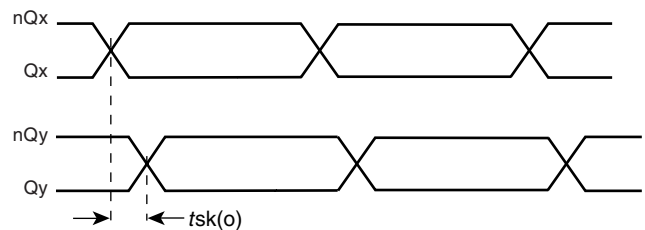
OUTPUT LOAD AC TEST CIRCUIT



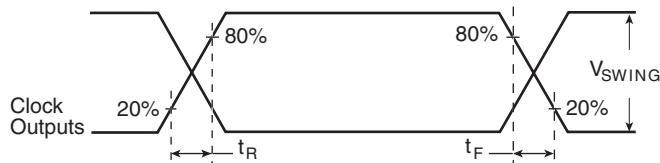
DIFFERENTIAL INPUT LEVEL



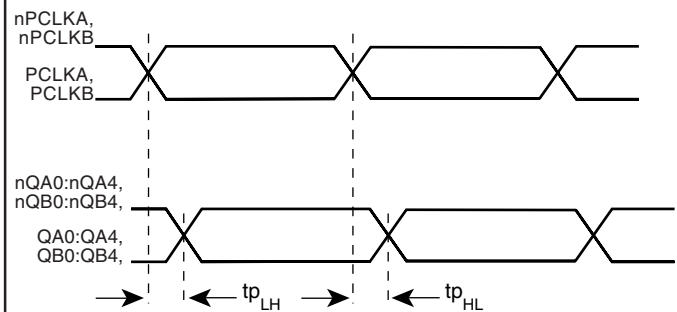
PART-TO-PART SKEW



OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVPECL LEVELS

Figure 1A shows an example of the differential input that can be wired to accept single ended levels. The reference voltage level V_{BB} generated from the device is connected to the

negative input. The C1 capacitor should be located as close as possible to the input pin.

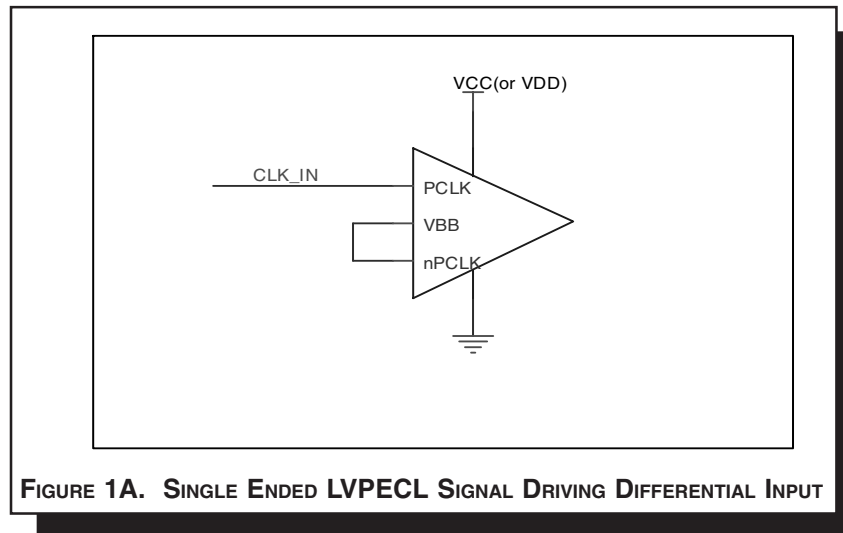


FIGURE 1A. SINGLE ENDED LVPECL SIGNAL DRIVING DIFFERENTIAL INPUT

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1B shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} \approx V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

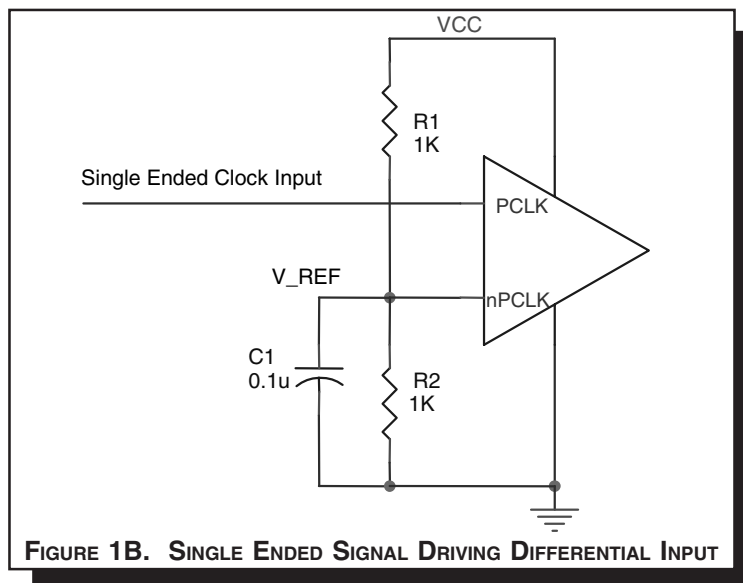


FIGURE 1B. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT



TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

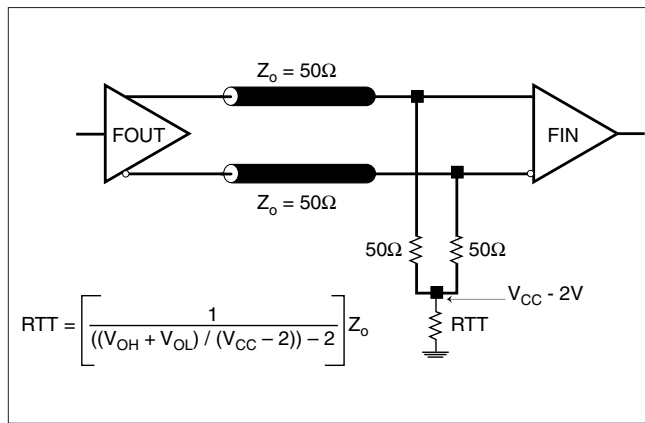


FIGURE 2A. LVPECL OUTPUT TERMINATION

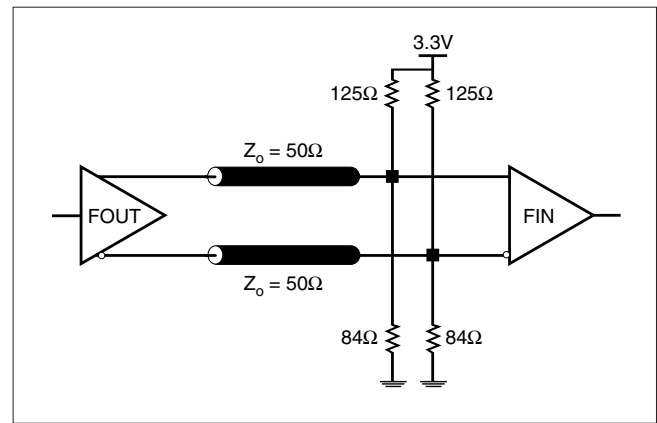


FIGURE 2B. LVPECL OUTPUT TERMINATION



TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 3A and Figure 3B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very close to

ground level. The R3 in Figure 3B can be eliminated and the termination is shown in Figure 3C.

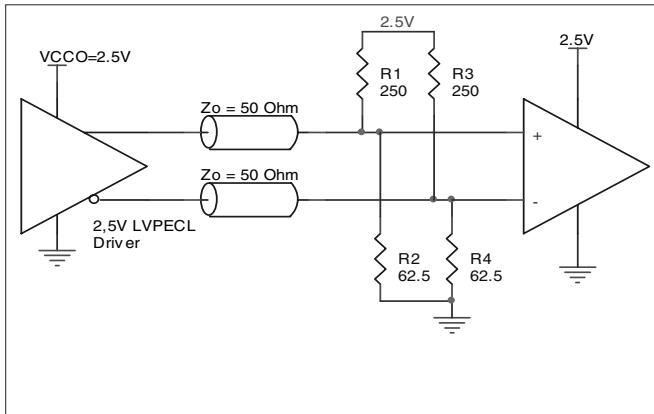


FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

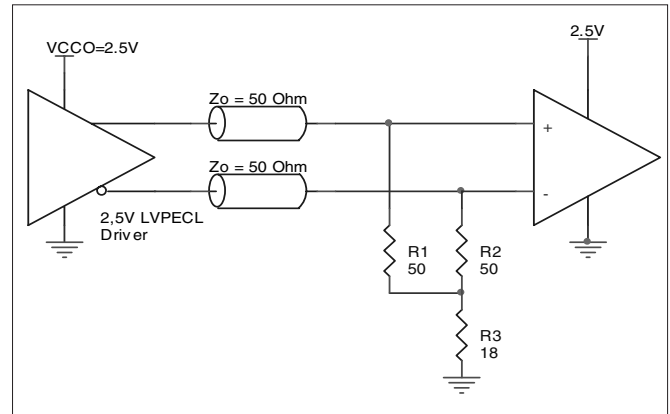


FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

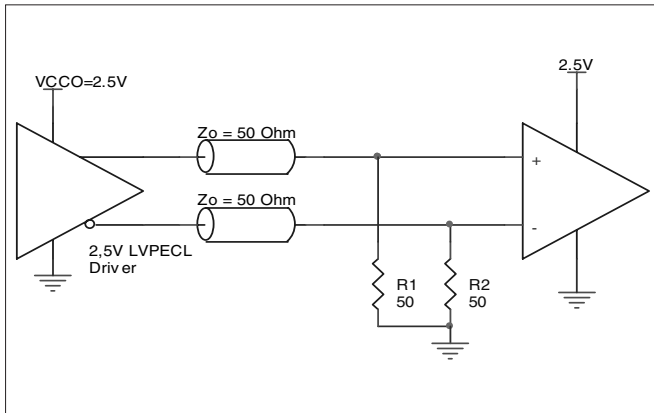


FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE



LVPECL CLOCK INPUT INTERFACE

The PCLKx/nPCLKx accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to 4E show interface examples for the HiPerClockS PCLKx/nPCLKx input driven by the most common driver types. The input interfaces

suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

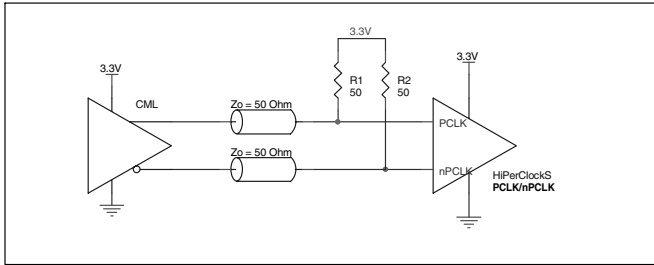


FIGURE 4A. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A CML DRIVER

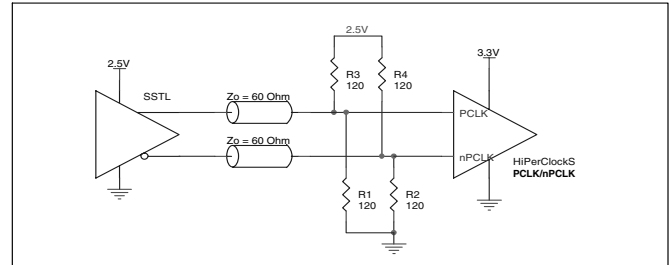


FIGURE 4B. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER

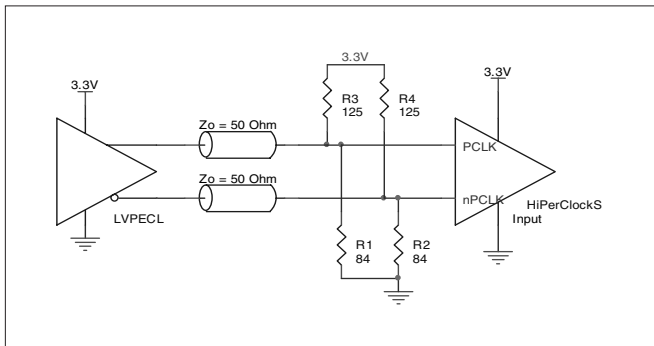


FIGURE 4C. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

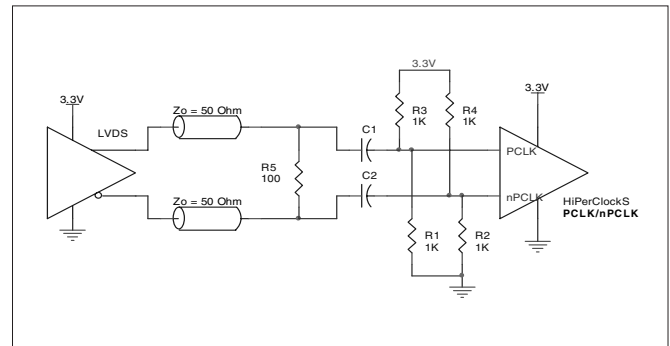


FIGURE 4D. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

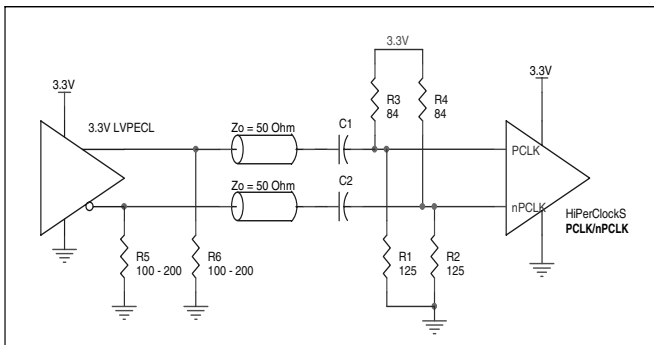


FIGURE 4E. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853210. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS853210 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.8V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.8V * 80mA = 304mW$
- Power (outputs)_{MAX} = **30.94mW/Loaded Output pair**
If all outputs are loaded, the total power is $10 * 30.94mW = 309.4mW$

Total Power_{MAX} (3.8V, with all outputs switching) = $304mW + 309.4mW = 613.4mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.613W * 42.1^\circ C/W = 110.8^\circ C$. This is well below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 32-PIN LQFP, FORCED CONVECTION

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|----------|------------|------------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 5.

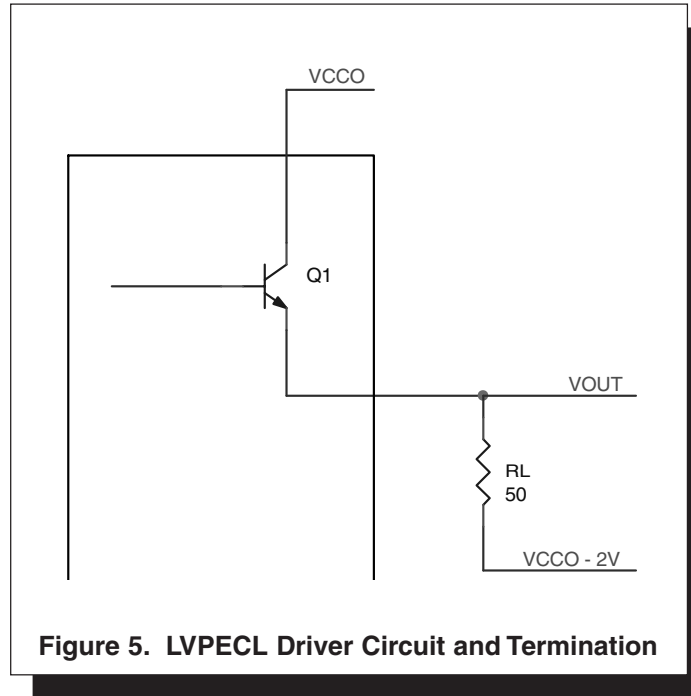


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.935V$

$$(V_{CC_MAX} - V_{OH_MAX}) = 0.935V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.67V$

$$(V_{CCO_MAX} - V_{OL_MAX}) = 1.67V$$

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.67V)/50\Omega] * 1.67V = 11.02mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30.94mW$$



RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|----------|------------|------------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS853210 is: 437



PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

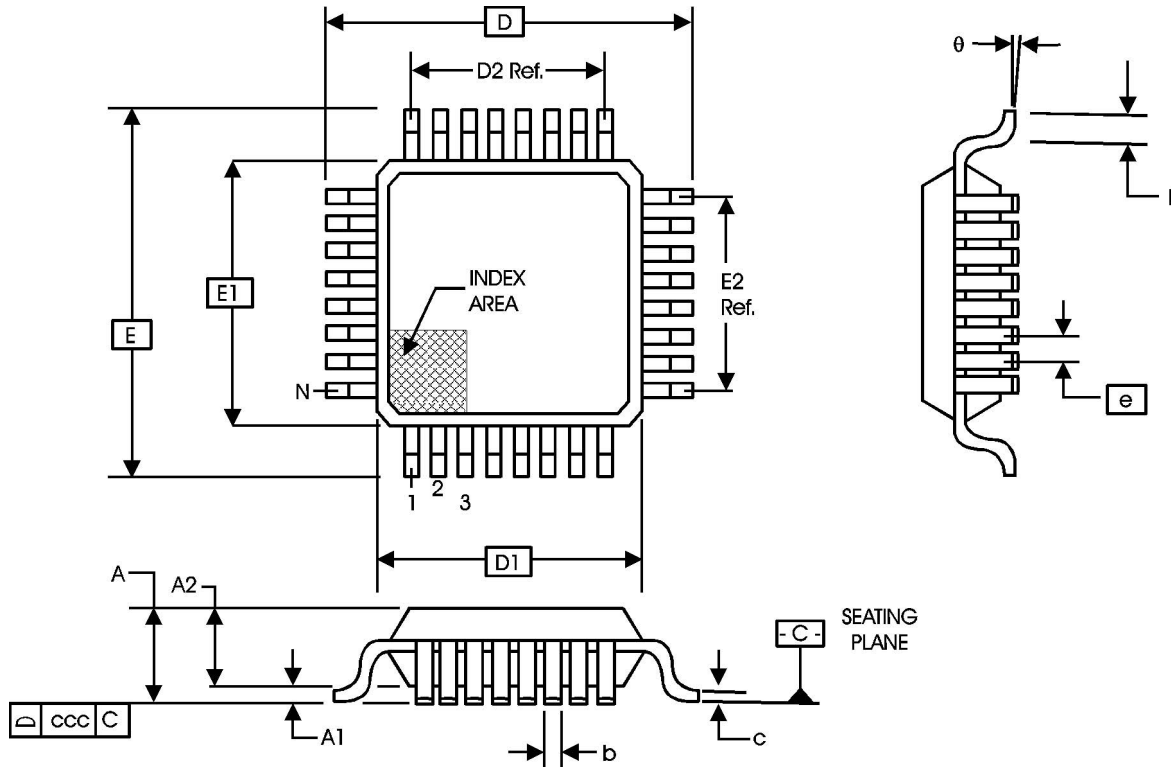


TABLE 7. PACKAGE DIMENSIONS

| JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | | |
|--|------------|---------|---------|
| SYMBOL | BBA | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | 32 | | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | -- | 0.20 |
| D | 9.00 BASIC | | |
| D1 | 7.00 BASIC | | |
| D2 | 5.60 Ref. | | |
| E | 9.00 BASIC | | |
| E1 | 7.00 BASIC | | |
| E2 | 5.60 Ref. | | |
| e | 0.80 BASIC | | |
| L | 0.45 | 0.60 | 0.75 |
| θ | 0° | -- | 7° |
| ccc | -- | -- | 0.10 |

Reference Document: JEDEC Publication 95, MS-026



Integrated
Circuit
Systems, Inc.

ICS853210

LOW SKEW, DUAL, 1-TO-5
DIFFERENTIAL-TO-2.5V/3.3V LVPECL/ECL FANOUT BUFFER

TABLE 8. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Count | Temperature |
|-------------------|-------------|-------------------------------|--------------|---------------|
| ICS853210AY | ICS853102AY | 32 lead LQFP | 250 per tray | -40°C to 85°C |
| ICS853210AYT | ICS853210AY | 32 lead LQFP on Tape and Reel | 1000 | -40°C to 85°C |

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